Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Currently amended) A power management method applied to a computer system, which is going to enter a power-saving mode, the computer system comprising a CPU, a north bridge communicating with the CPU according to a hyper transport I/O link protocol, a south bridge, a power supply, and at least one peripheral electrically connected to the north bridge, the method comprising the steps of:

enabling the CPU to output a power management signal to the south bridge via the north bridge;

enabling the south bridge to respond with a stop clock cycle to the CPU according to the power management signal;

enabling the CPU to respond with a stop grant message according to the stop clock signal;

enabling the north bridge to receive the stop grant message and analyze a power supply mode in the stop grant message, and enabling the north bridge to output a state transition signal to the at least one peripheral if the power supply mode is to suspend a main power supplied from the power supply;

enabling the at least one peripheral to respond with an acknowledge signal after the at least one peripheral finishes its state transition according to the state transition signal;

enabling the north bridge to pass the stop grant message to the south bridge after the north bridge receives the acknowledge signal;

enabling the south bridge to output a power control signal after the south bridge receives the stop grant message; and

enabling the power supply to suspend a corresponding power after the power supply receives the power control signal;

wherein the north bridge comprises a decoding unit for analyzing the power supply mode in the stop grant message; and the power supply mode is identified by analyzing, by the decoding unit, a system management action field (SMAF) in the stop grant message.

2. (Original) The power management method according to claim 1, wherein the at least one peripheral is a PCI express peripheral.

3. (Original) The power management method according to claim 2, wherein the PCI express link is transited from a state L0 to another state of L2/L3 ready according to the received state transition signal output from the north bridge.

4-5. (Canceled)

6. (Currently amended) A computer system with power management, the computer system comprising:

a CPU;

a north bridge comprising a decoding unit, the north bridge communicating with the CPU according to a hyper transport I/O link protocol;

a south bridge communicating with the CPU via the north bridge;

a power supply; and

at least one peripheral electrically connected to the north bridge, wherein:

when the computer system has to enter a power-saving mode, the CPU outputs a power management signal to the south bridge via the north bridge;

the south bridge then responds with a stop clock cycle to the CPU according to the power management signal;

the CPU then responds with a stop grant message according to the stop clock signal;

the north bridge then receives the stop grant message;

the decoding unit ~~analyzing~~ analyzes a power supply mode in the stop grant message, wherein the decoding unit analyzes a system management action field (SMAF) in the stop grant message to identify the power supply mode;

the north bridge outputs a state transition signal to the at least one peripheral if the power supply mode is to suspend a main power supplied from the power supply;

the at least one peripheral then responds with an acknowledge signal according to the state transition signal;

the north bridge passes the stop grant message to the south bridge after receiving the acknowledge signal;

the south bridge then receives the stop grant message and outputs a power control signal accordingly; and

the power supply then receives the power control signal and suspends a corresponding power accordingly.

7. (Original) The computer system according to claim 6, wherein the at least one peripheral is a PCI express peripheral.

8. (Original) The computer system according to claim 7, wherein the PCI express peripheral is transited from a state L0 to another state of L2/L3 ready after it receives the state transition signal output from the north bridge.

9. (Canceled)

10. (Currently amended) A power management method applied to a computer system, which is going to enter a power-saving mode, the computer system comprising a CPU, a north bridge communicating with the CPU according to a hyper transport I/O link protocol, a south bridge, a power supply, and at least one peripheral electrically connected to the north bridge, the method comprising the steps of:

(a) requesting to enter a power-saving mode, step (a) comprising:

outputting a power management signal;

responding with a stop clock cycle according to the power management signal; and

responding with a stop grant message according to the stop clock signal;

(b) determining whether or not to inform the at least one peripheral to transit its state according to a packet of the hyper transport I/O link protocol, step (b) comprising:

receiving the stop grant message;

analyzing a power supply mode in the stop grant message, and outputting a state transition signal to the at least one peripheral if the power supply mode is to suspend a main power supplied from the power supply, wherein the power supply mode is identified by analyzing a system management action field (SMAF) in the stop grant message; and

passing the stop grant message; and

(c) suspending a corresponding power according to the power-saving mode.

11. (Canceled)

12. (Original) The power management method according to claim 11, wherein the CPU outputs the power management signal to the south bridge via the north bridge.

13. (Original) The power management method according to claim 11, wherein the south bridge outputs the stop clock cycle to the CPU according to the power management signal.

14. (Original) The power management method according to claim 11, wherein the CPU responds with a stop grant cycle according to the stop clock signal.

15. (Original) The power management method according to claim 11, wherein the packet of the hyper transport I/O link protocol is the stop grant message.

16. (Canceled)

17. (Currently amended) The power management method according to ~~claim 16~~ claim 11, wherein the at least one peripheral is a PCI express peripheral.

18. (Original) The power management method according to claim 17, wherein the PCI express peripheral is transited from a state L0 to another state of L2/L3 ready after it receives the state transition signal output from the north bridge.

19. (Canceled)

20. (Original) The power management method according to claim 10, wherein the step (b) is performed by the north bridge.

21. (Original) The power management method according to claim 10, wherein the step (c) comprises:

outputting a power control signal according to the stop grant message; and

suspending the corresponding power according to the power control signal.

22. (Original) The power management method according to claim 21, wherein the south bridge outputs the power control signal.

23. (Original) The power management method according to claim 21, wherein the power supply suspends the corresponding power.